Direct Transistor-level Layout For Digital Blocks

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Cell-based design methodologies have dominated layout generation of digital circuits. Unfortunately, the growing demands for transparent process portability, increased performance, and low-level device sizing for timing/power are poorly handled in a fixed cell library. Direct Transistor-Level Layout For Digital Blocks proposes a direct transistor-level layout approach for small blocks of custom digital logic as an alternative that better accommodates demands for device-level flexibility. This approach captures essential shape-level optimizations, yet scales easily to netlists with thousands of devices, and incorporates timing optimization during layout. The key idea is early identification of essential diffusion-merged MOS device groups, and their preservation in an uncommitted geometric form until the very end of detailed placement. Roughly speaking, essential groups are extracted early from the transistor-level netlist, placed globally, optimized locally, and then finally committed each to a specific shape-level form while concurrently optimizing for both density and routability. The essential flaw in prior efforts is an over-reliance on geometric assumptions from large-scale cell-based layout algorithms. Individual transistors may seem simple, but they do not pack as gates do. Algorithms that ignore these shape-level issues suffer the consequences when thousands of devices are poorly packed. The approach described in this book can pack devices much more densely than a typical cell-based layout.Direct Transistor-Level Layout For Digital Blocks is a comprehensive reference work on device-level layout optimization, which will be valuable to CAD tool and circuit designers. EAN/ISBN : 9781402080630 Publisher(s): Springer Netherlands, Springer US Format: ePub/PDF Author(s): Gopalakrishnan, Prakash - Rutenbar, Rob A.

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