

Introduction To Noise-resilient Computing - , Seiya Kasai

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Noise abatement is the key problem of small-scaled circuit design. New computational paradigms are needed, as these circuits shrink, they become very vulnerable to noise and soft errors. In this lecture, we present a probabilistic computation framework for improving the resiliency of logic gates and circuits under random conditions induced by voltage or current fluctuation. Among many probabilistic techniques for modeling such devices, only a few models satisfy the requirements of efficient hardware implementation; specifically, Boltzman machines and Markov Random Field (MRF) models. These models have similar built-in noise immunity characteristics based on feedback mechanisms. In probabilistic models, the values 0 and 1 of logic functions are replaced by degrees of beliefs that these values occur. An appropriate metric for degree of belief is probability. We discuss various approaches for noise-resilient logic gate design, and propose a novel design taxonomy based on implementation of the MRF model by a new type of binary decision diagram (BDD), called a cyclic BDD. In this approach, logic gates and circuits are designed using 2-to-1 bi-directional switches. Such circuits are often modeled using Shannon expansions with the corresponding graph-based implementation, BDDs. Simulation experiments are reported to show the noise immunity of the proposed structures. Audiences who may benefit from this lecture include graduate students taking classes on advanced computing device design, and academic and industrial researchers. Author: Yanushkevich, Svetlana N. Author: Kasai, Seiya Author: Tangim, Golam Publisher: Morgan & Claypool Publishers Illustration: N Language: ENG Title: Introduction to Noise-Resilient Computing Pages: 00120 (Encrypted PDF) On Sale: 2013-01-01 SKU-13/ISBN: 9781627050227 Category: Technology & Engineering : Electronics - Circuits - General

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