# Multicore Systems On-chip



Conventional on-chip communication design mostly use ad-hoc approaches that fail to meet the challenges posed by the next-generation MultiCore Systems on-chip (MCSoC) designs. These major challenges include wiring delay, predictability, diverse interconnection architectures, and power dissipation. A Network-on-Chip (NoC) paradigm is emerging as the solution for the problems of interconnecting dozens of cores into a single system on-chip. However, there are many problems associated with the design of such systems. These problems arise from non-scalable global wire delays, failure to achieve global synchronization, and difficulties associated with non-scalable bus-based functional interconnects. The book consists of three parts, with each part being subdivided into four chapters. The first part deals with design and methodology issues. The architectures used in conventional methods of MCSoCs design and custom multiprocessor architectures are not flexible enough to meet the requirements of different application domains and not scalable enough to meet different computation needs and different complexities of various applications. Several chapters of the first part will emphasize on the design techniques and methodologies. The second part covers the most critical part of MCSoCs design - the interconnections. One approach to addressing the design methodologies is to adopt the so-called reusability feature to boost design productivity. In the past years, the primitive design units evolved from transistors to gates, finite state machines, and processor cores. The network-on-chip paradigm offers this attractive property for the future and will be able to close the productivity gap. The last part of this book delves into MCSoCs validations and optimizations. A more qualitative approach of system validation is based on the use of formal techniques for hardware design. The main advantage of formal methods is the possibility to prove the validity of essential design requirements. As formal languages have a mathematical foundation, it is possible to formally extract and verify these desired properties of the complete abstract state space. Online testing techniques for identifying faults that can lead to system failure are also surveyed. Emphasis is given to analytical redundancy-based techniques that have been developed for fault detection and isolation in the automatic control area. EAN/ISBN : 9789491216336 Publisher(s): Springer, Berlin, Atlantis Press Format: ePub/PDF Author(s): Abderazek,

Ben Abadallah



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