

Low Power Networks-on-chip

[DOWNLOAD HERE](#)

1;Preface;8 2;About the Editors;14 3;Contents;16 4;Contributors;18 5;Part I Low-Level Design Techniques;22 5.1;Chapter 1 Hybrid Circuit/Packet Switched Network for Energy Efficient on-Chip Interconnections;23 5.1.1;1.1 Network on-Chip: Past, Present, and the Future;23 5.1.1.1;1.1.1 State of the Art in NoCs;24 5.1.1.1.1;1.1.1.1 Buses;24 5.1.1.1.2;1.1.1.2 Rings;24 5.1.1.1.3;1.1.1.3 Meshes;25 5.1.1.2;1.1.2 Issues and Challenges for the Future;25 5.1.1.2.1;1.1.2.1 Power and Energy;25 5.1.1.2.2;1.1.2.2 Heterogeneity;26 5.1.2;1.2 Proposed Hybrid Packet/Circuit Switched NoC;27 5.1.2.1;1.2.1 Circuit-Switched Data with Packet-Switched Arbitration NoC;27 5.1.2.2;1.2.2 Circuit Innovations for Circuit/Packet Switched Network Arbitration;30 5.1.2.3;1.2.3 Data Transmission Circuit Innovations;33 5.1.3;1.3 NoC Measurements and Tradeoffs in 45nm CMOS;35 5.1.4;1.4 Conclusion;39 5.1.5;References;39 5.2;Chapter 2 Run-Time Power-Gating Techniques for Low-Power On-Chip Networks;41 5.2.1;2.1 Introduction;41 5.2.2;2.2 On-Chip Virtual-Channel Router;42 5.2.2.1;2.2.1 Target Router Architecture;42 5.2.2.2;2.2.2 Power Analysis of the Target Router Architecture;44 5.2.3;2.3 Previous Work on Low-Power Techniques;45 5.2.3.1;2.3.1 Voltage and Frequency Scaling Techniques;45 5.2.3.2;2.3.2 Power Gating Techniques;46 5.2.3.2.1;2.3.2.1 Coarse-Grained Power-Gating Techniques;46 5.2.3.2.2;2.3.2.2 Fine-Grained Power Gating Techniques;46 5.2.3.2.3;2.3.2.3 Power Gating for Interconnection Networks;47 5.2.4;2.4 Fine-Grained Power Gating Router;48 5.2.4.1;2.4.1 Power Domain Partitioning;48 5.2.4.2;2.4.2 Power Domain Implementation;49 5.2.4.3;2.4.3 Wakeup Latency Estimation;50 5.2.5;2.5 Wakeup Control Methods;51 5.2.5.1;2.5.1 Wakeup Latency Impact;51 5.2.5.2;2.5.2 Look-Ahead Method;52 5.2.5.3;2.5.3 Look-Ahead with Ever-On Method;54 5.2.5.4;2.5.4 Look-Ahead with Active Buffer Window Method;54 5.2.6;2.6 Experimental Evaluations;55 5.2.6.1;2.6.1 Simulation Environment;55 5.2.6.2;2.6.2 Performance Impact;57 5.2.6.3;2.6.3 Leakage Power Reduction;59 5.2.7;2.7 Summary;60 5.2.8;References;62 5.3;Chapter 3 Adaptive Voltage Control for Energy-Efficient NoC Links;64 5.3.1;3.1 Introduction;64 5.3.2;3.2 Methods for Energy-Efficient On-Chip Links;65 5.3.2.1;3.2.1 Metrics for Energy Efficiency;65 5.3.2.2;3.2.2 Datalink Layer Techniques;66 5.3.2.2.1;3.2.2.1 Bus Invert and Extended Bus Invert Coding;66 5.3.2.2.2;3.2.2.2

Frequent Value Coding;66 5.3.2.2.3;3.2.2.3 Crosstalk Avoidance Coding;67 5.3.2.2.4;3.2.2.4 Asymptotic Zero-Transition Coding;67 5.3.2.3;3.2.3 Physical Layer Techniques;68 5.3.2.3.1;3.2.3.1 Low-Swing Signaling;68 5.3.2.3.2;3.2.3.2 Differential Signaling;69 5.3.2.3.3;3.2.3.3 Repeater Insertion;69 5.3.2.3.4;3.2.3.4 Dual-Voltage Buffers;70 5.3.2.3.5;3.2.3.5 Pulsed Transmission;70 5.3.2.3.6;3.2.3.6 Current Mode Signaling;71 5.3.2.3.7;3.2.3.7 Globally Asynchronous Locally Synchronous (GALS) Signaling;71 5.3.2.3.8;3.2.3.8 Quasi-Resonant Interconnect;71 5.3.2.3.9;3.2.3.9 Adaptive Link Voltage Scaling;72 5.3.2.4;3.2.4 Other Methods;72 5.3.2.4.1;3.2.4.1 Integrating Double Sampling with Adaptive Voltage Scaling;72 5.3.2.4.2;3.2.4.2 Combining Error Control Coding with Adaptive Voltage Scaling;72 5.3.3;3.3 Lookahead-Based Transition-Aware Link Voltage Control;73 5.3.3.1;3.3.1 Lookahead Transmitter Design;74 5.3.3.2;3.3.2 HI/LO Voltage Selection;77 5.3.3.3;3.3.3 Performance Evaluation;78 5.3.3.3.1;3.3.3.1 Comparison with Traditional Two-Inverter Driver;79 5.3.3.3.2;3.3.3.2 Comparison with Adaptive Voltage Driver;81 5.3.3.3.3;3.3.3.3 Comparison with Prior Dual-Voltage Switching Method;83 5.3.3.4;3.3.4 Limitations;84 5.3.4;References;86 5.4;Chapter 4 Asynchronous Communications for NoCs;89 5.4.1;4.1 Introduction;90 5.4.1.1;4.1.1 Variability;91 5.4.1.2;4.1.2 Power Consumption;92 5.4.1.3;4.1.3 Chapter Structure;93 5.4.2;4.2 History of Asynchronous Communications Before the NoC Era;94 5.4.3;4.3 Token-Based EAN/ISBN : 9781441969118 Publisher(s): Springer, Berlin, Springer Science & Business Media Discussed keywords: Embedded Systems, Network-on-Chip (NoC), Niederspannung Format: ePub/PDF Author(s): Silvano, Cristina - Lajolo, Marcello - Palermo, Gianluca

[DOWNLOAD HERE](#)

Similar manuals:

[Advances In Design And Specification Languages For Embedded Systems](#)

[Advances In Design Methods From Modeling Languages For Embedded Systems And SoC's](#)

[Design Methodologies For Secure Embedded Systems](#)

[Design Technology For Heterogeneous Embedded Systems](#)

[Embedded Systems For Smart Appliances And Energy Management](#)

[Embedded Systems Specification And Design Languages](#)

[Enhancing Embedded Systems Simulation](#)

[From Model-Driven Design To Resource Management For Distributed Embedded Systems](#)

[Languages For Embedded Systems And Their Applications](#)

[Memory Controllers For Real-Time Embedded Systems](#)

[Pro Linux Embedded Systems](#)

[Radiation Effects On Embedded Systems](#)

[Solutions On Embedded Systems](#)

[Spatial Awareness Of Autonomous Embedded Systems](#)

[System-Level Design Techniques For Energy-Efficient Embedded Systems](#)

[Views On Evolvability Of Embedded Systems](#)

[Memory Allocation Problems In Embedded Systems](#)

[Embedded Systems](#)

[Multiplexed Networks For Embedded Systems](#)

[How To Land A Top-Paying Embedded Systems Software Developers Job: Your Complete Guide To Opportunities, Resumes And Cover Letters, Interviews, Salari - Rachel Matthews](#)

[FreeBSD For Developers - Develop Embedded Systems Ver 2011](#)

[Chapter 23, Specifying Behavior Of Embedded Systems - Robert Oshana](#)

[Chapter 03, Overview Of Real-time And Embedded Systems - Robert Oshana](#)

[Chapter 01, DSP In Embedded Systems: A Roadmap - Robert Oshana](#)

[Chapter 04, Overview Of Embedded Systems Development Lifecycle Using DSP - Robert Oshana](#)